TMT ANALYTICS

Weebit Nano Limited

ReRAM Memory provides the best of both worlds

Weebit Nano (ASX:WBT) is developing a memory technology, which we believe has the potential to complement and even partially replace DRAM and Flash memory within three to five years' time, in applications such as data centers, smart phones, laptops and IoT devices. The market for these two memory technologies is expected to total US$ 100BN in 2017.

Data is eating the world and we need more capacity to store it all

Driven by fast growth of mobile and IoT devices, autonomous vehicles, Artificial Intelligence, personal assistants etc., data and video is being generated at an exponentially growing rate. Storing and processing all this information today is mostly done using Flash memory and DRAM, which are very old semiconductor technologies. Going forward, the fast-rising costs to scale down DRAM memory cells well below 20 nanometers (nm) will become inhibitive. Additionally, achieving more than 128 layers in 3D NAND Flash is currently considered a significant challenge since etching through multiple layers while depositing the NAND string Flash cells in ever higher aspect ratios will be at the expense of manufacturability and reliability.

In other words, cost effective density improvements in NAND Flash and DRAM are expected to run out of steam in the next three to five years.

Hybrid memory technology to sit in between Flash and DRAM

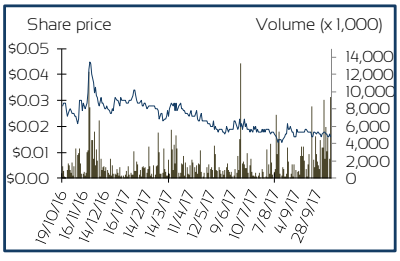
Enter ReRAM (Resistive RAM), which can be considered a hybrid memory technology, i.e. non-volatile like Flash memory, but approximately as fast as DRAM. WBT is developing Silicon Oxide (SiOx) ReRAM, which will sit between Flash and DRAM where performance metrics are concerned.

Fast, versatile, low energy and CMOS compatible

WBT's technology has several key advantages over certain other emerging memory technologies. SiOx has been used in semiconductor manufacturing for decades and is a very well-understood material that the semiconductor industry knows how to process. Therefore, SiOx ReRAM is CMOS compatible and should have a relatively short time-to-market once licensed to a semiconductor manufacturer.

The technology is versatile and suitable for use in both embedded memory, such as in IoT devices, as well as Systems on a Chip (SoC). Furthermore, we believe Storage Class Memory (SCM) will be a major application area for SiOx ReRAM as well.

Number of shares (m)	1342.3
Number of shares FD (m)	1422.6
Market capitalisation (A$ m)	22.8
Free Float (%)	57%
12 month high/low A$	0,045/0,014
Average daily volume (k)	1,699



Company report

ASX:WBT

Semiconductors & Semiconductor Equipment

Australia

Risk: High

Founded in Israel in 2015, Weebit Nano Ltd (WBT) is developing a newly emerging computer memory technology that combines the best of today's mainstream memory technologies, i.e. DRAM and Flash memory. Non-volatile like Flash and nearly as fast as DRAM, WBT's SiOx ReRAM will likely be able to complement and partially replace DRAM and Flash if and when the technology can be commercialized in a few years' time.

BUY

Current price: A$ 0.017

Price target: A$ 0.07

19 October 2017

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Power consumption is very low given the significantly reduced switching voltage, down to about CMOS voltage levels (<3.3V), which avoids the use of power hungry charge pumps, while access speeds are about 1,000x faster than Flash memory.

Significant achievements to date

WBT has already built Kb arrays of memory cells at 300nm and has demonstrated fast write speeds (100x to 1,000x faster than NAND Flash), low energy consumption, narrow resistivity distribution across the arrays and zero cell-to-cell interference at this resolution.

The achievement of narrow resistivity distribution across the arrays is particularly important as it shows uniformity across a large number of cells, which is crucial in validating the ability to scale up the technology to Mb and, eventually, Gb arrays.

Additionally, the achievement of Kb arrays in itself is very significant as this implies WBT should be able to build Mb and Gb arrays as well, given that these simply comprise of many individual Kb arrays.

Clear development milestones for the next nine months

The next step for the company will be to scale down the technology from the current 300nm resolution to 40nm, which it hopes to achieve in the fourth quarter of 2017 to be followed by test cells in Kb and Mb arrays at 40nm resolutions in the first half of 2018. We believe WBT's key challenge in the next 9 to 12 months will be to achieve performance uniformity across Mb arrays of its SiOx ReRAM cells at 40nm.

Collaboration with LETI has substantially accelerated the development process

Shortly after listing in August 2016, WBT engaged CEA/LETI in France to collaborate on the development of its SiOx ReRAM technology. Since then, WBT's development progress has been remarkable with the company expecting to achieve 40nm memory cell resolutions before year-end 2017. Without this development partner, the company would have needed to raise substantially more capital, in our view.

New CEO with strong commercialization background

CEO Coby Hanoch was appointed per 1 October 2017 and has been active in the Semiconductor industry for 37 years, including an eleven-year stint at National Semiconductor. Mr. Hanoch was also part of the founding team of Verisity, an electronics design verification software company, where he was responsible for worldwide sales. Verisity was sold to Cadence Design Systems (NASDAQ: CDNS) in 2005 for US$315M. Cadence is one of the leading providers of Electronic Design Automation (EDA) tools for semiconductor design. Combined with Chairman Perlmutter's Intel pedigree, we believe Mr. Hanoch's profile is well suited to WBT's upcoming commercialization phase of the company's lifecycle.

Discussions around IP licensing should trigger rerate of the shares

Once all of the technical development milestones have been hit, expected by mid-2018, we believe WBT will be in a position to start concrete discussions with memory players, foundries and IDM's to licence the technology on a non-exclusive basis.

In our view, these discussions should be the trigger for a substantial rerate of WBT's valuation, i.e. initially towards valuations seen for more commercially advanced ASX-listed semiconductor peers such as BrainChip (ASX:BRN) and BluGlass (ASX:BLG). These two companies have an average market cap A$ 139M.

Price target of A$ 0.07 per share with further upside potential

We believe WBT should be able to initially rerate towards A$ 100M, or A$ 0.07 per share, while the longer-term potential may be substantially higher than that, driven by the potential to agree multiple IP licenses as well as by potential M&A speculation once the technology becomes a bit more mature.

Starting coverage with BUY rating

Given the substantial commercial potential of WBT's SiOx ReRAM technology, we start our coverage of WBT with a BUY recommendation and an initial price target of A 0.07 per share.

New memory type to address future memory requirements

Weebit Nano (ASX:WBT) is developing a newly emerging type of computer memory technology, called Resistive RAM or ReRAM, that should be able to complement and/or partially replace existing memory technologies, such as DRAM and NAND Flash memory in a few years' time.

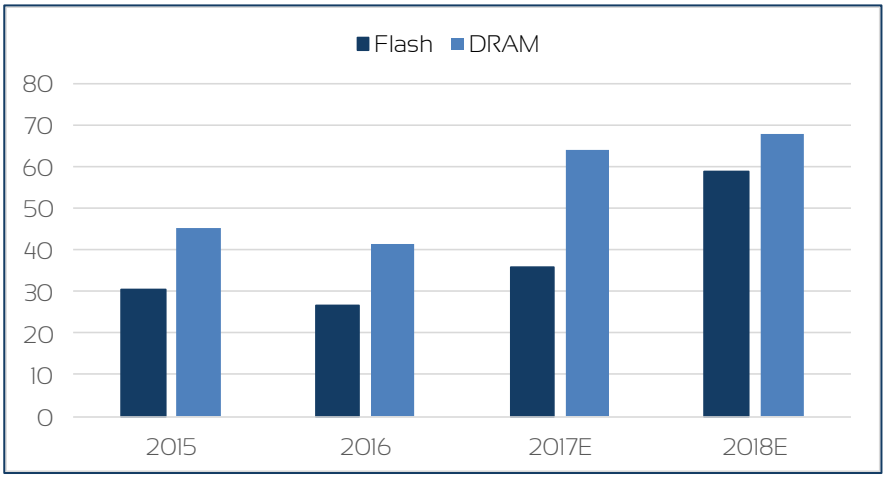
While DRAM is a very fast type of memory medium, it is also volatile, meaning that the memory cell will lose its stored information once the electrical power is switched off. Flash memory, on the other hand, will retain stored information without power, but is up to 1,000x slower than DRAM.

DRAM and Flash worth about US$ 100BN in 2017

Both of these memory types play a very significant role in today's electronics, with the latest laptop and desktop computers utilizing both DRAM and Flash memory in large quantities. Additionally, fast growth in data center capacity and fast increasing memory capacity in mobile devices, such as smart phones, tablets and digital cameras, is providing additional impetus for unit growth in Flash memory consumption.

These trends are clearly reflected in today's market growth trends. The global market for DRAM is expected to amount to US$ 64BN in 2017 according to IC Insights. This implies 55% growth compared to 2016. The value of the NAND Flash market is expected to grow by 35% in 2017 to an estimated US$ 36BN.

FIGURE 1: FLASH MEMORY AND DRAM MARKET SIZE (IN US$BN)



Source: TMT Analytics, IC Insights

Increasingly hard to further miniaturize computer chips

However, while growth for both memory types is expected to remain high through the semiconductor cycle in the next five years, a scaling problem is on the horizon. In the past 50 years, rapidly developing semiconductor manufacturing techniques have helped scale down computer chips to resolutions (electrical circuitry linewidths) that measure less than 15 nanometers (nm) for the most advanced logic chips, such as Intel's i9 processors (1 millimeter is 1,000,000 nanometers).

Today's most advanced NAND Flash memory chips are manufactured at 40nm resolutions in 3D structures, i.e. stacked on top of each other, like apartments in a skyscraper. The most advanced DRAM chips are manufactured at resolutions below 20nm.

It is expected that further downscaling of memory chips will become increasingly difficult from a technological stand point. As memory cell sizes become smaller and smaller, there is increasing likelihood of current leakage, where memory cells lose part of their stored electrical charge due to thinner cell walls. Additionally, adjacent cells can start to suffer from so-called cross talk, i.e. interference with the adjacent memory cells. These effects result in read errors when the value of the particular cell is read out.

WBT addressing the sweet spot between DRAM and Flash

We expect that leading-edge logic chips, such as Intel's and AMD's, will become commercially available at 10nm or below in 2018 and can possibly go as low as 7nm within a few years' time.

However, the fast-rising costs to scale down DRAM memory cells well below 20nm will become inhibitive. Additionally, achieving more than 128 layers in 3D NAND Flash is currently considered a significant challenge since etching through multiple layers while depositing the NAND string Flash cells in increasingly high aspect ratios will be at the expense of manufacturability and reliability. In other words, cost effective density improvements in NAND Flash and DRAM are expected to run out of steam in the next three to five years.

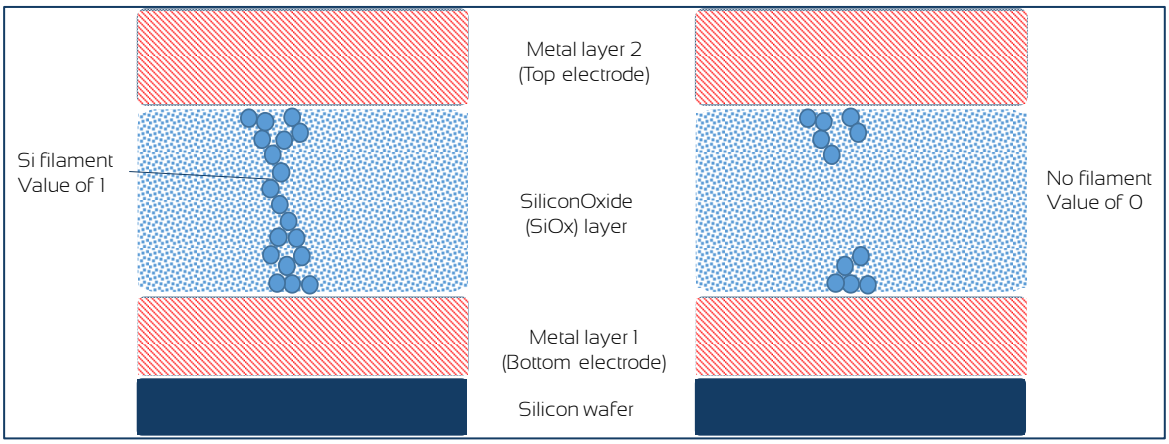
> *Enter ReRAM, which can be considered a hybrid memory technology: non-volatile like Flash memory, but approximately as fast as DRAM.*

ReRAM is based on resistance rather than electrical charge

The values of 1 and 0 in NAND Flash memory cells are attributed based on the trapped electrical charge that is present in the memory cell's floating gate. The cells are charged and read by applying an electrical current to them.

A ReRAM cell, on the other hand, is attributed a value of 1 or 0 based on the resistance level of the cell material that is sandwiched in between two electrodes. A value of 1 is attributed to a state of low resistivity, while a value of 0 is attributed to a state of high resistivity.

FIGURE 2: CELL SWITCHING BY FORMING AND BREAKING A SILICON FILAMENT IN A SIOX SWITCHING LAYER



Source: TMT Analytics

Manipulating the cell resistance levels by creating a filament

Changing the resistance level of a ReRAM cell can be done through interface switching, which changes the resistivity of the entire layer in between the electrodes, or by creating a filament that connects the two electrodes of the memory cell. WBT uses the latter technology.

Very good prospects to embed SiOx ReRAM memory cells in logic chips

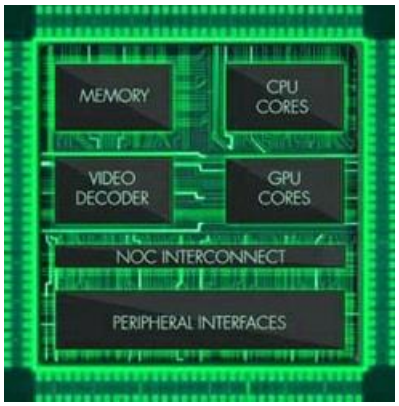
The technology WBT is developing is based on the forming of a conductive channel between the two metal electrodes of a ReRAM cell. These electrodes are typically made out of metals, such as titanium, tungsten, aluminum or copper. The conductive channel is formed inside a non-conductive Silicon Oxide (SiOx) layer.

SiOx has typically been used as an insulating component in semiconductor manufacturing. However, by applying a certain voltage to one of the electrodes, a switchable conductive pathway of silicon nanowires (filament) can be formed within the SiOx layer (see Figure 2). In this high conductivity, low resistance state, the cell value is 1. By subsequently applying a reverse voltage to the electrode, the filament can be broken down again, effectively switching the memory cell back to the original state of 0.

The actual filament is formed as the applied electrical voltage strips away some of the oxygen atoms in the SiOx layer, leaving the silicon atoms to cluster and form a conductive silicon pathway to the other electrode. The size of the filament is approximately 5nm to 7nm in diameter.

> *The filament diameter is very small and can potentially bring certain major advantages to semiconductor manufacturers if and when SiOx ReRAM is commercialized. Specifically, the potential to embed WBT's memory technology into logic chips and entire systems (System on a Chip, or SoC, see Figure 3) can present very substantial commercial opportunities.*

FIGURE 3: SOC CONFIGURATION



Source: Siteservice.info

SiOx ReRAM has several key advantages

SiOx ReRAM has some very distinct advantages compared to other emerging memory technologies, such as PCM (Phase Change Memory), FRAM (Ferroelectric RAM), STT-RAM (Spin transfer torque RAM) and MRAM (Magneto resistive RAM).

CMOS compatibility means less manufacturing changeover for future licensees

Firstly, WBT's SiOx ReRAM technology is CMOS compatible. In other words, the cells can be manufactured using existing semiconductor manufacturing processes, materials and equipment. CMOS stands for Complementary Metal Oxide Semiconductor and is the predominant technology used to manufacture integrated circuits today.

Unlike some other technologies, such as PCM-based 3D XPoint, SiOx ReRAM doesn't require the use of novel materials in semiconductor fabs given that the material has been used in semiconductor manufacturing for decades. In turn, this doesn't require semiconductor manufacturers to develop new processes or purchase new manufacturing equipment, since the cells can be manufactured with existing deposition tools, specifically existing ALD (Atomic Layer Deposition), CVD (Chemical Vapor Deposition), PVD (Physical Vapor Deposition) and PECVD (Plasma Enhanced CVD) tools. This type of equipment is used to develop and grow the individual layers computer chips are made of.

This better manufacturability of WBT's memory cells not only means that potential licensees of the technology can keep using their existing manufacturing processes and semiconductor manufacturing equipment, but that they can also keep using existing supply chains for materials.

Overall, CMOS compatibility of WBT's technology means fewer manufacturing changeovers are required, which implies lower tooling costs for potential licensees of the technology. In addition, it can take years and significant efforts to get new machines to achieve the yield rates expected for production manufacturing. We believe this will be particularly interesting for semiconductor foundries (outsourcing companies for chip manufacturing) as these foundries typically process smaller production runs than Integrated Device Manufacturers (IDMs), such as Intel, STMicro, Samsung etc.

IDMs typically have production lines dedicated to certain products, used for high volume production during longer periods of time. Foundries, on the other hand, typically have much smaller production runs for their customers, and need to switch over to different product line setups quite frequently. Hence, they prefer to use standard equipment, materials and processes that are used industry-wide, rather than novel or exotic methods.

> *Consequently, we believe SiOx ReRAM will likely have broad appeal to semiconductor foundries, mostly based in Taiwan and China, looking for future SoC and embedded memory solutions for their customers.*

ReRAM can be up to 1,000x faster than today's Flash memory

Flash memory speeds are typically around 50,000 nanoseconds (ns), whereas DRAM speeds are typically between 13ns and 15ns (for DDR3 DRAM). Various ReRAM technologies, including Filamentary and Interface Switching ReRAM, are achieving speeds that are approaching DRAM speeds, i.e. more than 1,000x faster than Flash memory.

This is in part achieved by faster write speeds and less need for error correction post-write, given that ReRAM isn't based on electrical charges, unlike Flash memory. These electrical charges in

Flash memory cells can leak away and interfere with adjacent cells, which requires Flash memory cells to be checked for errors, which substantially limits the read speeds that can be achieved with Flash memory.

PCM typically also requires quite some error correction, putting ReRAM in a fairly good competitive position when it comes to future applicability of the technology.

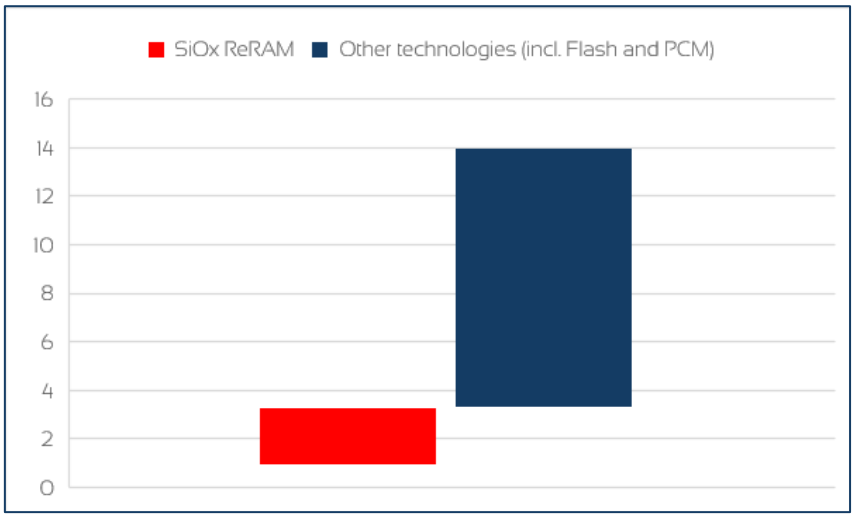
Substantially lower power consumption

WBT is using low voltage levels to set and reset its memory cells, whereas today's NAND Flash memory and certain other emerging memory technologies, such as PCM, use voltages between 3.3V and 14V (Figure 4).

ReRAM's lower energy consumption profile is of particular importance for mobile applications (smart phones, laptops, wearables etc), remote sensors as well as certain applications in data centers that require high frequency read/write cycles.

Therefore, we believe ReRAM has great applicability in these areas, i.e. both as embedded memory and as Storage Class Memory (SCM). SCM is high capacity computer memory, i.e. GB capacity, used in applications such as cloud and data center storage as well as mobile phones and laptops, that require low energy consumption and high endurance rates.

FIGURE 4: SWITCHING VOLTAGES FOR DIFFERENT TECHNOLOGIES (IN VOLTS)



Source: TMT Analytics

Small filament may result in good integration with logic functions in SoC's

The small diameter of the filament (5nm to 7nm) in the SiOx layer potentially allows for substantial downscaling of the memory cell and surrounding circuitry. Given that today's leading-edge resolutions of logic chips, such as CPU's, measure less than 20nm, downscaling of SiOx ReRAM cells to, say, 20nm-28nm, may more easily enable integration of this technology into SoC's and devices with embedded memory.

> *Put differently, the smaller the size of the memory cells, the closer they can be positioned to the logic elements on the chip in SoC's. This increases the chip speed, reduces power consumption and enables further device shrink.*

Smaller feature sizes should also allow future SiOx ReRAM cells to be stacked in 3D structures, similar to 3D NAND Flash today, to create higher bit densities at lower costs.

However, the crucial part in scaling down SiOx ReRAM cells below 30nm, and potentially even further towards 20nm, will be WBT's ability to scale down the chip circuitry around the actual memory cell. As the cell is scaled down, this surrounding circuitry will still need to be able to conduct the same voltages needed to switch the memory cell. If this circuitry gets too small, there may be a risk that the currents get too high and the circuitry will fail.

This issue will only come into play once WBT starts development work to scale its technology down below 40nm, which is not an immediate priority at the moment.

Very rapid development progress made to-date

Even though WBT has started development work on its technology only two years ago, when it licensed the key technology from Rice University in the United States (see appendix for more background), the progress to-date has been very substantial.

The company initially set out to transfer the technology to the facilities of its development partner LETI in Grenoble, France. We will elaborate on this partnership below. WBT subsequently aimed to manufacture initial, working memory cells at 300nm resolution, which is has achieved.

Low energy consumption

Initial characterization of the 300nm cells confirms that switching voltages are indeed at CMOS level, i.e. well below voltages required by Flash memory and some other emerging memory technologies.

High uniformity and write speeds

Furthermore, WBT has achieved high uniformity across a range of many different memory cells, e.g. required switching voltages, which is important in the eventual discussions with potential licensees. Furthermore, the company has confirmed write speeds that are approximately 1,000x faster than Flash memory. While error correction is expected to be minimal post-write, given the absence of an electrical charge in the cells, further characterization will still need to confirm this.

Endurance expected to be in excess of 100,000 write/erase cycles

One of the major drawbacks of NAND Flash technology is that its endurance is being degraded over scalability by design, up to the point that a technology once used to endure one million write and erase cycles is not guaranteed for more than 1,000-10,000 cycles today. This may be fine for the average smart phone or laptop, but it limits the application areas and, as individual cells start to fail, it implies a rapid decline of available memory capacity of the device over time.

Other emerging ReRAM technologies have demonstrated endurance cycles in excess of 100,000 cycles and we expect WBT will be able to achieve similar numbers at both 300nm and 40nm, and potentially substantially higher.

Achieved solid results in 300nm kilobit arrays

WBT has outlined several key milestones it expects to achieve through the middle of 2018. The company has already achieved 4Kb (kilobit) memory arrays at 300nm, which demonstrated uniformity of various performance metrics across 4x 1,024 individual cells, including narrow resistivity distribution across the arrays, low power consumption, fast write speeds (100x to 1,000 faster than NAND Flash) and zero cell-to-cell interference. Additionally, a test wafer showed 100% yield across certain arrays, meaning zero failure in initializing the cells in those arrays and in subsequent switching (writing and resetting) cycles.

> *The achievement of narrow resistivity distribution across the arrays is particularly important as it shows uniformity across a large number of cells, which is crucial in validating the ability to scale up the technology to Mb and, eventually, Gb arrays.*
>
> *Additionally, the achievement of Kb arrays in itself is very significant as this implies WBT should be able to build Mb and Gb arrays as well, given that these simply comprise of many individual Kb arrays.*

The next step: 40nm is the magic number

In parallel to the development of the Kb arrays at 300nm, WBT has been developing individual cells at 40nm resolution, a process it aims to complete by the end of 2017. 40nm is a crucial number in the development of newly emerging memory technologies as today's 3D Flash memory chips are manufactured at this resolution.

The idea is that if a new technology can be scaled down to 40nm, it can realistically be used to build 3D structures and be at par with Flash memory with respect to bit density. At this resolution, other metrics, such as energy consumption, speed and endurance should all be better than Flash memory, of course, in order to make the switch to a new technology worthwhile.

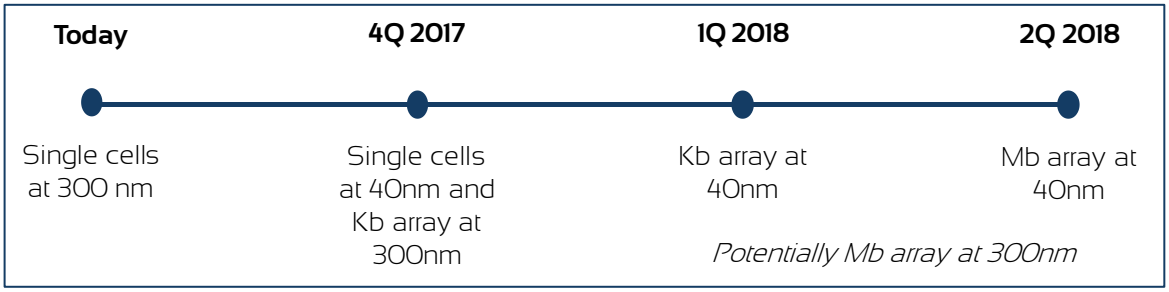
> *In practice though, we believe many of the newly emerging memory technologies, including SiOx ReRAM, will be able to scale well beyond 40nm in the next few years. The Netherlands-based ASML, the world's leading lithography equipment manufacturer, anticipates single level ReRAM cells will be patterned at 10nm resolution in 2TB chips by the time they become commercially available.*

Kb and Mb arrays at 40nm

A next step for WBT will be to develop Kb arrays at 40nm and demonstrating cell uniformity at the 40nm node across many thousands of memory cells (Figure 5). Because the company has already achieved 4Kb arrays at 300nm, we believe a Kb array at 40nm will likely be a fairly straightforward process. Given the pace of the development progress to-date and the current parallel development of 40nm single cells and 4Kb arrays at 300nm, we would expect WBT to be able to achieve Kb arrays at 40nm early in 2018.

WBT will subsequently move on to Megabit (Mb) arrays at 40nm, demonstrating further scalability of memory capacity. In a commercial environment, any future licensee will eventually want to scale up to Gb arrays at 40nm or below for SCM applications. Embedded memory and SoC applications will likely require lower capacity memory chips, e.g. Mb chips for certain IoT devices, sensors and automotive and industrial applications.

FIGURE 5: WEEBIT NANO TECHNOLOGY ROADMAP



Source: TMT Analytics

Key technical challenges in next few quarters

Summarizing the above, several key challenges need to be overcome in the next several quarters:

- Scaling down to 40nm from 300nm currently
- Achieve Kb arrays and Mb arrays at 40nm, and potentially at 300nm.
- Achieve uniformity in forming the atomic structure of the silicon filament in the SiOx layer across many different cells, i.e. location, width and the way the silicon atoms are arranged.

Longer term, we believe WBT's key development challenge will be to scale the surrounding cell architecture down with the core cell resolutions, e.g. towards 28nm. However, this is potentially a development challenge that a future licensee of WBT's SiOx ReRAM technology may undertake. It's not in the company's current development scope.

Collaboration with LETI to expedite the development process

Shortly after its RTO in August 2016, WBT engaged LETI in France to collaborate on the development of its SiOx ReRAM technology. LETI is a well-renowned research institute in the field of micro- and nanotechnologies, specialized in bringing fundamental research projects into commercial environments. In other words, moving Intellectual property (IP) from lab to fab.

LETI have state-of-the-art facilities, including substantial clean room areas and advanced 200mm and 300mm semiconductor manufacturing equipment. LETI's experience in developing emerging memory technologies, such as ReRAM, dates back more than ten years during which time LETI has gained substantial expertise in Embedded memories for IoT and SoC applications as well as in SCM.

Furthermore, LETI has strong inroads into global semiconductor companies including key embedded memory and logic manufacturers, such as Intel, GlobalFoundries and STMicroelectronics, who we believe can be potential future licensees of WBT's technology.

Additionally, LETI partners with equipment manufacturers, such as Applied Materials (AMAT). AMAT is one of the world's leading suppliers of CVD and PVD equipment and we suspect this connection to LETI will be very beneficial for WBT's specific process development, which can be done using existing equipment and is based on existing manufacturing processes.

Collaborations such as the WBT/LETI one typically involve both partners sharing workloads in the areas of process development, integrations, reviews and data analysis.

Very attractive ROI from LETI engagement

While WBT has not disclosed the costs of retaining LETI, we believe a substantial part of the company's A$ 1M R&D expenditures in FY17 can be attributed to LETI. From an ROI point of view, we believe the engagement with LETI is very attractive considering the rapid progress WBT has made in the last twelve months. This progress would not have been possible had WBT set out on this development journey on its own, given the substantial costs of semiconductor equipment and clean room facilities. Without this development partner, the company would have needed to raise substantially more capital, in our view.

Commercialisation strategy focused on IP licensing

While technology development companies are typically engaged in strategic conversations with other industry players all the time, we believe WBT will need to hit certain technical milestones first before such conversation can become more serious and concrete.

Specifically, we believe the company will initially need to demonstrate:

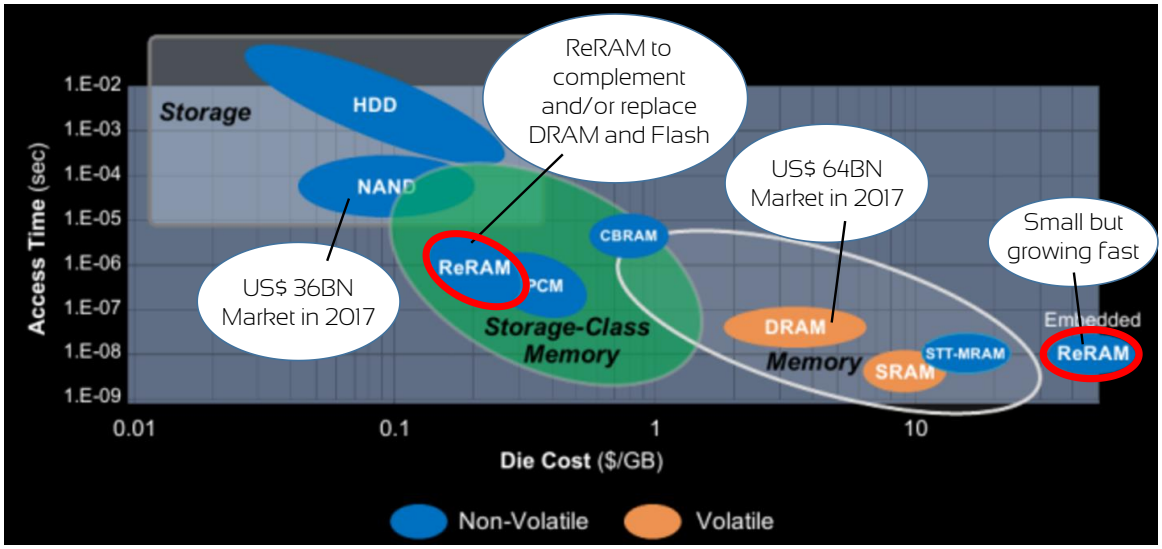
- Mb arrays of working memory cells at 40nm resolution,
- Of high performance uniformity,
- With minimal endurance of 100,000 Program/Erase (PE) cycles,
- At read speeds below 100ns,
- Using a low switching voltage (we anticipate <3.3V),
- And simulated data retention of several years.

> *Timing wise, we would expect WBT to be in a position to engage in serious commercial discussions from mid-2018 onwards, when we expect the company to have achieved most, if not all, of these milestones.*

Target markets include Storage Class Memory and Embedded memory/SoC

Generally, the specific performance metrics of future memory chips can be fine-tuned depending on the specific application. E.g. for SCM applications, performance metrics of the memory chips can be optimized for use in data centers (high data retention), mobile applications (high endurance) etc. However, today's main memory types, DRAM and Flash, are commoditized, meaning memory devices from different memory manufacturers can be used interchangeably, while pricing is fairly transparent, especially for DRAM. We expect a certain level of commoditization in SCM devices as well, once they become mainstream.

FIGURE 6: THE MARKET OPPORTUNITY FOR RERAM



Source: Western Digital, TMT Analytics

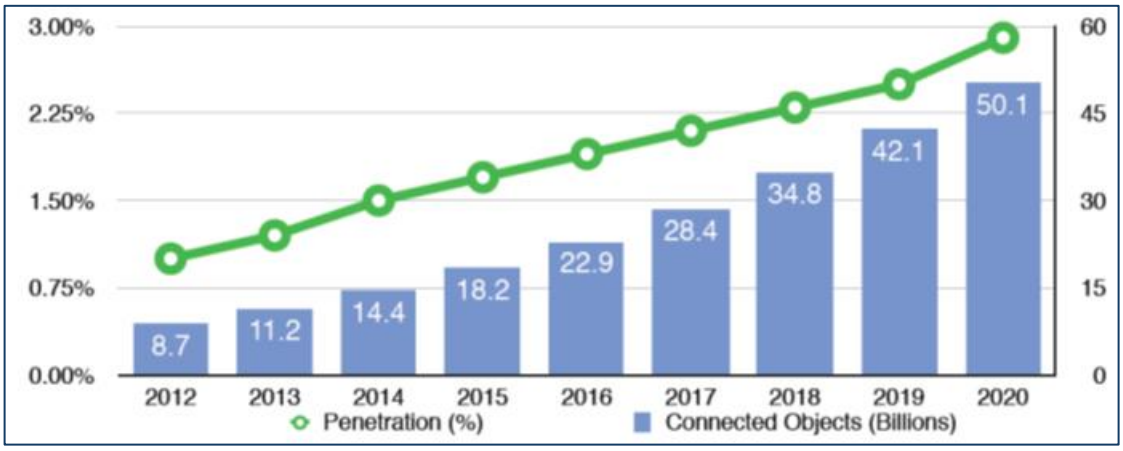
The most attractive market for WBT's technology will be embedded memory IoT devices and SCM, in our view, given the large size as well as the opportunity to co-exist with DRAM and Flash. Moreover, as scalability of existing technologies becomes a more pressing issue in the next few years, we believe there will also be substantial room to replace DRAM and particularly Flash for certain applications.

Embedded memory market expected to grow very fast

As discussed earlier, embedded memories are integrated into electronics devices, such as microcontrollers, sensors etc. Embedded Flash (eFlash) and embedded Erasable Programmable Read Only Memory (eEPROM) are some of the main types of embedded memory.

Fast growth of the Internet of Things (IoT) implies fast growth of the embedded memory market since IoT devices, used in smart homes, smart parking, wearables, connected cars, robotics etc, all require some form of energy efficient, low latency memory. Even though these memory requirements are typically much lower than for SCM, i.e. Kb and Mb capacity rather than GB and TB, the sheer number of IoT nodes (50BN by 2020 according to Cisco, Figure 7), will likely lead to extremely fast unit growth of embedded memory chips going forward, in our view.

FIGURE 7: CISCO'S PROJECTIONS FOR GROWTH OF IOT DEVICES



Source: Cisco

Additionally, the fast growth of the IoT drives the rapid integration of wireless communication technologies, such as Near Field Communication (NFC), Bluetooth and ZigBee into many electronic devices. And wireless communication requires embedded memory.

Lastly, ongoing industrial automation and the emergence of autonomous vehicles will also strongly drive demand for embedded memory.

Likely commercial partners

When looking at the different addressable markets for ReRAM, we believe SK Hynix, Western Digital, Samsung and Panasonic are likely candidates to potentially be interested in licensing WBT's technology for SCM applications.

Some of the key players in the embedded memory market include, Microchip Technology, HHGrace, Kilopass, eMemory Technology and SST, which we believe will likely be interested in adopting ReRAM as a next-gen embedded memory technology.

In addition, we believe semiconductor foundries, such as TSMC, UMC, SMIC and GlobalFoundries will generally be interested in offering ReRAM technologies to customers, especially for embedded memory and SoC applications at high resolutions, i.e. with logic elements <16nm.

We make specific mention of STMicro in France as a potential licensee, given LETI's strategic relationship with this semiconductor manufacturer that is active in both logic and embedded memory.

Multiple monetization scenarios are possible

Given the very substantial costs (US$ 300M to US$ 500M) to develop semiconductor IP through to commercialization and the costs to build and run a semiconductor fab (> US$ 1BN), which are excessive for smaller companies, WBT's strategy is to develop SiOx ReRAM to the point where established semiconductor manufacturers consider the technology commercially feasible. At that time, WBT will aim to monetize the technology commercially.

When it comes to monetizing on semiconductor IP, the industry typically takes a very pragmatic approach reflected in three possible scenarios for WBT:

1) IP licensing involves payment of a one-off license fee and subsequent royalty payments to the IP owner. Royalty payments are typically based on a percentage of the selling price of the chip that includes the licensed IP, ranging from 5% to 20%. Occasionally, the IP owner will receive payments for Non-Recurring Engineering work on behalf of the licensee, e.g. specific integration work. IP licensing can be exclusive (single licensee) or non-exclusive (multiple parties can license the technology).

2) Through an outright acquisition of the IP-owning entity, a semiconductor company can acquire the company's entire IP portfolio, including all patents. This way, the acquiring company has exclusive rights to use the specific IP.

   Even though patent owner Rice University can theoretically block an acquisition of WBT, it would be in their best interest if WBT were to be acquired by a semiconductor manufacturer as this would broaden the use of their patents, and would consequently maximize the cash return on these patents.

3) A third, less used option, is strategic partnering, where an IP development company teams up with an established industry player, e.g. with a major memory player to jointly market a new technology. While this set up can work to initially bring a new technology to market, we believe established semiconductor companies prefer more direct control and ownership in cases where the new technology presents very high potential.

We believe a best-case scenario for WBT would be if the company were able to license its technology to multiple licensees on a non-exclusive basis, for instance to multiple foundries, pure memory players and SoC/embedded memory manufacturers.

At the same time, we wouldn't rule out a strategic acquisition of WBT by an industry player looking to exclusively use the company's technology.

License fees and royalty payments in non-exclusive license deals are usually substantially lower compared to payments in exclusive license agreements. However, non-exclusive licensing will enable WBT to sign multiple licensees and have an open-ended revenue upside.

Valuation should be about potential and technology milestones

Pre-revenue Tech companies' valuations are typically driven by the longer term commercial potential of the technology and their near to medium term development progress. The former depends on factors such as addressable market size, growth, sector incumbents and particularly the potential of the innovative/disruptive nature of the technology being developed. The near to medium term development progress should be measurable through company announcements in which technical development milestones are announced and referenced back to the company's development roadmap.

The balance, or weight, between the two will depend on individual investors' preferences, investment profiles and investors' patience levels. On aggregate though, we would say that early stage Tech stocks listed in the US and Europe tend to have investor bases that put more weight on the longer-term potential of the technologies being developed than on near term milestones that need to be hit.

> *We believe the key reason for this is that US and European investors generally have a better understanding of technology and can see beyond the development milestones that Tech companies need to achieve in order to unlock the longer-term potential of the technology. As a consequence, Tech companies listed in these markets tend to be valued at levels that reflect this long-term potential.*

ASX-listed tech stocks suffer from "proof-of-the-pudding" syndrome

ASX-listed Tech companies, on the other hand, typically have an investor base that is more than 90% Australian. And given that Australian investors' background in technology is generally less developed compared to those of Tech investors in the US, Europe and Asia, we find that local investors oftentimes struggle to see the long-term potential of certain emerging technologies.

In other words, local investors actually need the milestones to verify that the company is on track to achieve that long-term potential, even though these milestones may be non-events for more experienced Tech investors overseas who are familiar with that specific technology and/or development processes in a particular technology sub-sector.

> *And even when Tech companies hit their key development milestones, which confirms they are on the right track to achieve their long-term potential, ASX-listed companies may still not rerate towards levels seen in more Tech-savvy markets given the extreme focus of Australian investors on revenues.*

In other words, whereas overseas' Tech investors invest in the potential of a technology, Australian investors tend to invest in the actual monetization of a technology, i.e. in a "proof of the pudding is in the eating"-type approach.

In our view, this "proof of the pudding" syndrome is particularly prevalent among ASX-listed Tech stocks in the semiconductors, data analytics/processing, artificial intelligence and micro systems subsectors.

Great investment opportunities for patient investors who know what to look for

This means that valuations of many high potential Tech stocks listed on the ASX are substantially lower than what they would likely be, had these stocks been listed in Tech-savvy stock markets overseas.

However, given the high potential of their respective technologies, there is a strong likelihood that these companies will be able to successfully license and/or sell their technology in due time. We expect some of these companies are even likely to be acquired by larger industry peers at some point.

Consequently, we believe great investment opportunities exist among the smaller ASX-listed Tech companies. Given the Proof-of-the-pudding syndrome though, capturing this value will require patience on the part of investors.

Proof-of-the-pudding syndrome clearly reflected in WBT's peer group

In our view, WBT's peer group (Figure 8) clearly reflects this Proof-of-the-pudding syndrome. Companies such as BrainChip (ASX:BRN) and BluGlass (ASX:BLG), that have developed highly promising technologies, which have resulted in initial commercial deals and collaborations with large industry players, are still valued very modestly when referenced to their commercial potential or potential takeout price.

When it comes to the ASX-listed memory players, including WBT, the picture is even more dramatic, with an average valuation of just A$ 23.7M. WBT is currently valued at A$ 22.8M.

FIGURE 8: WBT SEMICONDUCTOR PEER GROUP

Company	Code	Semiconductor sub sector	Share price	Market cap (fully dil., A$ M)
Strategic Elements	SOR	Nano cube memory	0.097	23.7
4DS Limited	4DS	Interface Switching ReRAM	0.029	24.5
BluGlass	BLG	Semiconductor equipment	0.36	137.7
Brainchip	BRN	Artificial Neural Networks	0.165	140.0
Weebit Nano	**WBT**	**SiOx ReRAM**	**0.017**	**22.8**

Source: TMT Analytics

US Venture capital demonstrates attractiveness of emerging memory tech

The average Venture Capital (VC) funding of emerging memory technology companies in the United States to-date amounts to approximately US$ 100M (Figure 9). VC funds typically only invest in new technology companies if the perceived exit value is an order of magnitude higher than their original investment.

FIGURE 9: VENTURE CAPITAL FUNDING FOR EMERGING MEMORY TECHNOLOGIES

Company	Technology	Funding to-date (US$ M)
Crossbar	ReRAM	81
Everspin	MRAM	81
Crocus Technology	MRAM	98
Spin Transfer Technologies	Spin Transfer Torque MRAM	106
Avalanche Technology	Spin Transfer Torque MRAM	107
Weebit Nano	SiOx ReRAM	10.8
4DS Memory*	Interface Switching ReRAM	16.7
	** excludes HGST's development expenses estimated at >US$ 15M*	

Source: CrunchBase, TMT Analytics

In other words, we believe the potential exit values of VC-owned memory Tech companies illustrate the attractiveness of emerging memory technologies from an investment point of view as well as the very substantial upside potential for WBT from today's valuation.

WBT's value driven by future licensing discussions

Assuming that the Proof-of-the-pudding syndrome for ASX-listed Tech stocks isn't going away anytime soon, we believe WBT's value will predominantly be driven by future licensing discussions with potential licensees. In turn, these will be facilitated by the company achieving its development milestones in the next nine months, such as the 4Kb arrays at 300nm recently achieved, i.e. Kb and Mb arrays at 40nm in 1HY18.

> *In other words, we believe a substantial rerating of WBT shares is likely within the next nine to twelve months, assuming the company can hit its development milestones in the next several quarters.*

Initial price target of A$ 0.07 per share

Assuming WBT will be able to hit its development milestones, enabling the company to engage in concrete commercial discussions with industry players, we believe the initial rerate of the shares should start to bring the company's valuation more in line with its more advanced ASX-listed sector peers BRN and BLG, which are currently valued at A$ 139M on average.

As this rerate will likely not happen overnight, our initial target valuation for WBT is A$ 100 M, or A$ 0.07 per share. However, we believe there may be further upside beyond this initial target, depending on how commercial discussions progress.

Conclusion

Once WBT achieves the technical milestones for SiOx ReRAM outlined in this report, we believe the company can engage in concrete discussions with potential licensees of its technology. We believe the company should be able to demonstrate this commercial viability by mid-2018. The key challenge in the next 9 to 12 months will be for WBT to achieve performance uniformity across Mb arrays of ReRAM cells at 40nm, i.e. filament formation, speed, data retention and endurance.

Monetization through IP licensing

In our view, the most likely monetization scenario will be non-exclusive licensing, i.e. multiple semiconductor companies paying WBT one-off license fees upfront and recurring royalties once computer chips using WBT's technology start being sold commercially, expected after 2020.

We start our coverage of WBT with a BUY recommendation and a price target of A$ 0.07 per share.

Near term share price drivers

- Achievement of single memory cells at 40nm, which is expected in 4Q17.
- Upscaling memory arrays to Kb arrays at 40nm and Mb arrays at 300nm, expected in 1Q18.
- Further upscaling to Mb arrays at 40nm, expected by mid-2018.

SWOT analysis

Strengths:

- Because of certain key characteristics, the SiOx ReRAM technology WBT is developing is a very strong contender in the race to complement and potentially partially replace DRAM and Flash memory in three to five years' time. In particular, the SiOx basis of the technology is a key strength, as it enables potential licensees to keep using currently existing manufacturing equipment, materials and production processes.
- The technology is protected with multiple patents.
- WBT's development partner, LETI, is well-renowned with a solid track record in development of SCM and embedded memory technologies.
- The technology infrastructure and eco-system in Israel is extremely well developed with most key players in the global semiconductor industry having a presence in the country, which will likely help WBT attract the right talent.
- The Intel pedigree of WBT's chairman, David Perlmutter, will likely be instrumental in developing highly relevant relationships with respect to the eventual licensing of WBT's technology or potential trade sale of the company.

Weaknesses:

- WBT doesn't directly own the patents underlying the technology, but licenses their use from Rice University in the United States. Rice University needs to keep valid and be able to defend its patents in case of infringements or challenges. We believe WBT has very little influence over these factors.
- Development of semiconductor technology requires substantial capital, which WBT will need to raise on a needs basis given its current cash position of around A$ 3M following the recent capital raise and its burn rate of approximately A$ 700k per quarter. This will result in dilution for existing shareholders and may need to be done under adverse market conditions.

Opportunities:

- The performance and metrics gap between DRAM and Flash memory leaves a very substantial opportunity for emerging memory technologies, such as SiOx ReRAM, to fill.
- The addressable SCM and embedded memory markets are very large (US$ 100BN in 2017 combined) and growing fast.
- We believe multiple global semiconductor companies will be looking to license or acquire ReRAM technology, such as SiOx ReRAM, once developed to the point of proven feasibility for commercial applications.

Threats:

- Deep-pocketed semiconductor companies may develop proprietary ReRAM or other emerging memory technologies, rendering WBT's technology obsolete and/or redundant.
- Capital markets conditions may turn negative, preventing WBT from raising sufficient capital, which may potentially inhibit the company in its technological development.
- The inherent cyclicality of the global semiconductor market may bring about potentially adverse conditions, such as falling DRAM and Flash memory prices that may lead potential licensees to push out licensing decisions around emerging memory technologies.

Appendices

Board members

David Perlmutter (Non-Executive Chairman): Mr. Perlmutter has nearly 40 years of experience in the semiconductor industry and is currently Managing General Partner in Eucalyptus Growth Capital, focusing on investment in growing technology companies in Israel. Prior to that, Mr. Perlmutter held an Executive Vice President and General Manager position at the Intel Architecture Group (IAG) and was chief product officer of Intel Corporation (NASDAQ: INTC) until 2014. Mr. Perlmutter received an award for innovation in industrial development from the Israeli president in 1987 for the development of the i387 math coprocessor and was elected a Fellow of the Institute of Electrical and Electronics Engineers (IEEE Fellow) for contributions to the mobile personal computer industry. Mr. Perlmutter is a member of the Board of Directors of Mellanox Technologies (NASDAQ: MLNX) and chairs different non-profit organizations. He is also a Member of the Board of Governors of the Technion Israel Institute of Technology and on the board of directors of various startups.

Coby Hanoch (CEO and Managing Director): New CEO Coby Hanoch was appointed per 1 October 2017 and has been active in the Semiconductor industry for 37 years, including an eleven-year stint at National Semiconductor. Mr. Hanoch also was part of the founding team of Verisity, an electronics design verification software company, where he was responsible for worldwide sales. Verisity was sold to Cadence Design Systems (NASDAQ: CDNS) in 2005 for US$315M. Cadence is one of the leading providers of Electronic Design Automation (EDA) tools for semiconductor design. Mr. Hanoch was also VP of Worldwide Sales at Jasper Design Automation, doubling their sales in 3 years and enabling the $170M acquisition by Cadence. Additionally, he was CEO of Packetlight, leading a turnaround for the company. In his most recent role as President and CEO of EDAcon Partners, Mr. Hanoch was focused on commercializing EDA (Electronic Design Automation) tools and Semiconductor Intellectual Property (IP).

Yossi Keret (Non-Executive Director): Mr. Keret has extensive managerial and financial experience and has led a variety of international companies in different fields including industrial, financing, biotech and high-tech startups both in Europe and the USA. Mr. Keret has vast experience in public and private companies and took a major part in M&A negotiations and implementation as well as in complex international tax planning. Mr. Keret has played a major part in Initial Public Offerings (IPO) on NASDAQ and has led successful private equity raising (PIPE) for public companies.

Kobi Ben-Shabat (Non-Executive Director): Mr. Ben-Shabat has vast experience in sales, senior management and building new companies from the ground up as a Board member in various companies. He was the founder and Managing Director of Open Platform Systems, which was founded in 2007, operated across Australia and New Zealand, and was acquired by Hills PTY LTD (ASX: HIL) in April 2014. Currently Mr. Ben-Shabat is the founder and CEO of Ultra charge (ASX: UTR).

Ananda Kathiravelu (Non-Executive Director): Mr. Kathiravelu has been in the financial services, funds management and stock broking industries for over 20 years. He holds a Bachelor of Business and a Graduate Diploma of Applied Finance and Investment. Mr. Kathiravelu is the Managing Director of Armada Capital Ltd, a corporate advisory company that provides strategic corporate advice and services to listed and unlisted companies. He is currently a non-executive director of Buddy Platform Ltd. (ASX : BUD). His areas of expertise include corporate advice, capital raising, mergers and acquisitions.

Ashley Krongold (Non-Executive Director): Mr. Krongold has spent 15 years in the Investment Banking and Accounting industries. He was a founding member of Investec Bank Australia and

is currently CEO of the Krongold Group and a non-executive director of Dotz Nano Ltd (ASX: DTZ). Mr. Krongold is also a founding General Partner of global equity crowd-funding platform, OurCrowd.

Advisory Board

Prof. James Tour is Professor of Materials Science and Nano Engineering and a Professor of Computer Science at Rice University in Houston, Texas. He is well known for his work in molecular electronics and molecular switching molecules. Prof. Tour holds more than 60 US patents and has published over 500 articles. He was named among "the 50 most Influential Scientists in the world today" in 2014 and was selected as Scientist of the Year by R&D magazine in 2013. Prof. Tour is co-applicant on multiple patents that WBT has licensed from Rice University.

SiOx ReRAM Technology

WBT has licensed the core SiOx ReRAM IP on an exclusive basis from Rice University in the United States, which owns the 6 underlying patents.

Rice University's patents

6 patents:

US 12/848,626

US 14/050,589

US 12/435,661

US 12/782,448

US 14/240,973

In filing - US 15/033,726

Key terms of the IP license agreement between WBT and Rice University

Rice University will receive 1.5% royalties of gross sales made by WBT. In case WBT sublicenses the technology, Rice University will receive 25% of any cash or non-cash consideration received by WBT.

Minimum royalty payments will amount to:

$10,000 per 1 January 2019,

$20,000 per 1 January 2020,

$100,000 per 1 January 2021,

$250,000 per 1 January 2022,

$500,000 per 1 January of each of the following years.

WBT has also agreed to sponsor research into 3D stackable Non-Volatile Memory by Rice university for three years up to 1 January 2018 for a total amount of $750,000. WBT has an option to license the IP generated by this research.

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